REMARKS

This is in response to the Final Office Action of September 8, 2003. Claims 25-44 were rejected. Claim 30 was amended. Claims 25-44 are pending.

Claims 30-36 were rejected under 35 U.S.C. §112 with the Examiner contending that the specification did not support the element of a transfer memory. Applicant respectfully disagrees, but has amended claim 30 to recite a transfer buffer in order to clarify the support for a transfer memory. Applicant's specification discloses an embodiment on page 8, lines 5-15 having a transfer buffer established in memory in which data describing a large number of vertices may be stored.

The Examiner rejected independent claim 25 as being anticipated by Fujimoto (U.S. Pat. No. 5,559,952). Claims 26, 27, and 37 were rejected as being obvious over Fujimoto. Claims 28-29 and 38-44 were rejected as being obvious over Fujimoto in view of Wada (U.S. Pat. No. 5,959,639). Claims 30-36 were rejected as being obvious over Fujimoto in view of Wada and Holt et al. (U.S. Pat. No. 5,760,792). Applicant respectfully traverses these rejections.

In section 2 of the Office Action, the Examiner characterized the frame buffer cache 141 of Fujimoto as storing vertex data and as having a cache controller for checking cached vertex data. Applicant respectfully disagrees with the Examiner's characterization of Fujimoto. Fujimoto caches a fundamentally different type of data and uses it for a fundamentally different purpose than in Applicant's claimed invention. Consequently, Applicant respectfully submits that Fujimoto cannot anticipate or render obvious Applicant's claimed invention.

Applicant's independent claims 25, 30, 37, and 41 include limitations corresponding to a cache having stored vertex data. The vertex cache of Applicant's claimed invention thus caches a specific type of data – vertex data – for use by the graphics module in rendering pixel data.

Vertex data is data identifying a point that marks the intersection of two or more edges of a polygon or other graphics object. Rendering is a specific graphics process associated with generating data for displaying pixels. A pixel is a picture element corresponding to a single element of a display. Extracts from Computer Graphics Dictionary, Ed. Roger T. Steven, Charles River Media, (2002) regarding some of the common definitions of vertex, pixel and rendering are attached for the convenience of the Examiner in understanding these technical distinctions.

Applicant's claimed invention thus caches a specific type of data – vertex data – that the graphics module can use to generate (render) pixels. However, while vertex data may be used in the process of generating pixels, vertex data (data regarding the intersection of edges of a polygon) is not pixel data (data for displaying an individual picture element of a display).

Applicant respectfully submits that Fujimoto teaches away from the element of a cache for storing vertex data. Instead, Fujimoto has a frame buffer cache 141 for caching pixel data as illustrated in Figure 1 of Fujimoto.

Fujimoto teaches in column 5, lines 58-59, that the frame buffer cache 141 of Fujimoto caches image data of the same type as frame buffer 30. (VRAM 30 is identified as a frame buffer in column 4, lines 42-44). The data stored in the frame buffer 30 (and hence in the frame buffer cache 141) is in the form of color information for individual pixels (see, e.g., column 4, lines 46-52). This is consistent with the common definition, as described in Computer Graphics Dictionary, that a frame buffer "contains memory to store the color of each pixel together with circuitry to manage input to the memory and output in a form that can be accepted by the monitor." A copy of this definition is attached for the convenience of the Examiner.

Regarding independent claims 25, 30, 37, and 41, these claims have a limitation corresponding to a vertex data stored in a cache for use by a graphics module to render pixels. However, since the frame buffer cache of Fujimoto stores pixel data, it cannot teach or suggest a limitation corresponding to caching vertex data.

Regarding independent claims 25, 30, 37, and 41, these claims recite limitations corresponding to checking (or reading) a cache for cached vertex data for a polygon. Fujimoto cannot perform this function. As previously described, the frame buffer cache of Fujimoto does not store vertex data and hence cannot teach or suggest a limitation corresponding to checking a cache for cached vertex data.

Regarding independent claims 25 and 30, these independent claims include limitations corresponding to a cache controller checking the vertex cache in response to a request for the graphics module to render a polygon. Fujimoto cannot perform this function. As previously described, the frame buffer cache of Fujimoto does not cache vertex data and hence cannot teach or suggest a cache controller performing this function.

Applicant thus respectfully submits that the independent claims are in condition for allowance. The dependent claims are allowable for at least the same reasons as the independent

claims from which they depend. Consequently, in view of the foregoing amendments and remarks, it is respectfully submitted that all pending claims in application are now in a condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No 03-3117.

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